WHAT IS CLAIMED IS:

1. A synchronous semiconductor memory device in which an operation of a row-system circuit is started in response to input of a first command and an operation of a column-system circuit is started in response to input of a second command, comprising:

a first circuit configured to generate a first signal for a normal operation mode based on a command detection signal which is activated in response to the first command,

a second circuit configured to receive the command detection signal, an operation mode specifying signal which selectively specifies one of the normal operation mode and test mode and a selection signal used to select at least part of the memory cells in a memory cell array and generate a second signal for a test mode to synchronize start timing of the operation of the row-system circuit with input timing of the second command, and

a third circuit configured to select the first signal output from the first circuit when the normal operation mode is specified by the operation mode specifying signal, select the second signal output from the second circuit when the test mode is specified, and generate a third signal used to activate at least part of the memory cells in the memory cell array based on a selected one of the first and second signals and the

selection signal.

2. A synchronous semiconductor memory device according to claim 1, wherein the second command is input in a cycle next to a cycle in which the first command is input.

3. A synchronous semiconductor memory device according to claim 1, wherein the second circuit includes a delay circuit which delays start timing of the operation of the row-system circuit with respect to the second command in one clock unit or half clock unit.

4. A synchronous semiconductor memory device according to claim 1, wherein the selection signal is a signal which selects a bank in the memory cell array and the third signal is a signal which activates the selected bank in the memory cell array.

5. A synchronous semiconductor memory device in which an operation of a row-system circuit is started in response to input of a first command and an operation of a column-system circuit is started in response to input of a second command, comprising:

a first circuit configured to generate a first signal for a normal operation mode based on a command detection signal which is activated in response to the first command,

a second circuit configured to receive the command detection signal, an operation mode specifying signal

which selectively specifies one of the normal operation mode and test mode and a selection signal used to select at least part of the memory cells in a memory cell array and generate a second signal for a test mode to synchronize start timing of the operation of the row-system circuit with the clock cycle time in which a column selection line is activated, and

a third circuit configured to select the first signal output from the first circuit when the normal operation mode is specified by the operation mode specifying signal, select the second signal output from the second circuit when the test mode is specified, and generate a third signal used to activate at least part of the memory cells in the memory cell array based on a selected one of the first and second signals and the selection signal.

6. A synchronous semiconductor memory device according to claim 5, wherein the second command is input in a cycle next to a cycle in which the first command is input.

7. A synchronous semiconductor memory device according to claim 5, wherein the second circuit includes a delay circuit which delays start timing of the operation of the row-system circuit with respect to the second command in one clock unit or half clock unit.

8. A synchronous semiconductor memory device

according to claim 5, wherein the selection signal is a signal which selects a bank in the memory cell array and the third signal is a signal which activates the selected bank in the memory cell array.

9. A synchronous semiconductor memory device in which an operation of a row-system circuit is started in response to input of a first command and an operation of a column-system circuit is started in response to input of a second command, comprising:

a first circuit configured to generate a first signal for a normal operation mode based on a command detection signal which is activated in response to the first command,

a second circuit configured to receive the command detection signal, an operation mode specifying signal which selectively specifies one of the normal operation mode and test mode and a selection signal used to select at least part of the memory cells in a memory cell array and generate a second signal for a test mode which sets start timing of the operation of the row-system circuit by sequentially delaying start timing of the operation of the row-system circuit with respect to the second command in one of a half-clock unit and one clock unit and selecting a delay amount based n a timing control signal, and

a third circuit configured to select the first signal output from the first circuit when the normal

operation mode is specified by the operation mode specifying signal, select the second signal output from the second circuit when the test mode is specified, and generate a third signal used to activate at least part of the memory cells in the memory cell array based on a selected one of the first and second signals and the selection signal.

10. A synchronous semiconductor memory device according to claim 9, wherein the second command is input in a cycle next to a cycle in which the first command is input.

11. A synchronous semiconductor memory device according to claim 9, wherein the second circuit includes a timing control circuit which selects a delay amount based on a timing control signal.

12. A synchronous semiconductor memory device according to claim 9, wherein the selection signal is a signal which selects a bank in the memory cell array and the third signal is a signal which activates the selected bank in the memory cell array.

13. A method for testing a synchronous semiconductor memory device in which an operation of a row-system circuit is started in response to input of a first command and an operation of a column-system circuit is started in response to input of a second command, comprising:

inputting an operation mode specifying signal

which selectively specifies one of a normal operation mode and test mode,

inputting a first command,

inputting a second command in a cycle next to a cycle in which the first command is input,

synchronizing start timing of the operation of the row-system circuit with input timing of the second command when the test mode is specified by the operation mode specifying signal,

activating at least part of memory cells in a memory cell array, and

making a screening test with respect to the activated memory cell.

14. A test method for the synchronous semiconductor memory device according to claim 13, wherein the second command is input in a cycle next to a cycle in which the first command is input.

15. A test method for the synchronous semiconductor memory device according to claim 13 in which the screening test having a guard band is made and which further comprises advancing switching timing of a column gating release signal for row-system control before making the screening test.

16. A method for testing a synchronous semiconductor memory device in which an operation of a row-system circuit is started in response to input of a first command and an operation of a column-system

circuit is started in response to input of a second command, comprising:

inputting an operation mode specifying signal which selectively specifies one of a normal operation mode and test mode,

inputting a first command,

inputting a second command in a cycle next to a cycle in which the first command is input,

synchronizing start timing of the operation of the row-system circuit with the clock cycle time in which a column selection line is activated when the test mode is specified by the operation mode specifying signal,

activating at least part of the memory cells in a memory cell array, and

making a screening test with respect to the activated memory cell.

17. A test method for the synchronous semiconductor memory device according to claim 16, wherein the second command is input in a cycle next to a cycle in which the first command is input.

18. A test method for the synchronous semiconductor memory device according to claim 16 in which the screening test having a guard band is made and which further comprises advancing switching timing of a column gating release signal for row-system control before making the screening test.

19. A method for testing a synchronous

semiconductor memory device in which an operation of a row-system circuit is started in response to input of a first command and an operation of a column-system circuit is started in response to input of a second command, comprising:

inputting an operation mode specifying signal which selectively specifies one of a normal operation mode and test mode,

inputting a first command,

inputting a second command in a cycle next to a cycle in which the first command is input,

delaying start timing of the operation of the row-system circuit with respect to the second command in one of a half-clock unit and one clock unit when the test mode is specified by the operation mode specifying signal,

selecting start timing of the operation of the row-system circuit based on a timing control signal,

activating at least part of the memory cells in a memory cell array, and

making a screening test with respect to the activated memory cell.

20. A test method for the synchronous semiconductor memory device according to claim 19, wherein the second command is input in a cycle next to a cycle in which the first command is input.

21. A test method for the synchronous

semiconductor memory device according to claim 19 in which the screening test having a guard band is made and which further comprises advancing switching timing of a column gating release signal for row-system control before making the screening test.